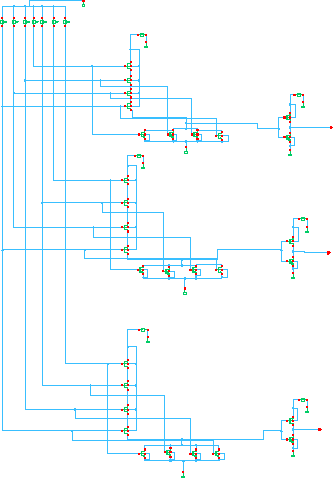
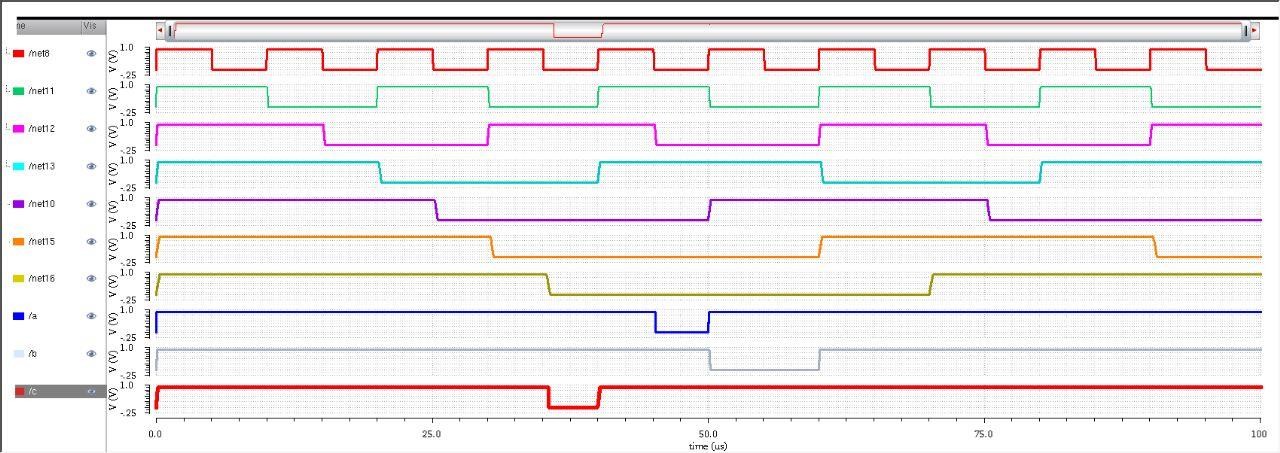
## Simulation Results

We have implemented basic combinational circuits required for 3-bit Flash ADC i.e., 8:3 Priority Encoder, Common Source Amplifier, Differential Amplifier and Comparator, and for sequential circuit Johnson Counter and D-Flipflop.

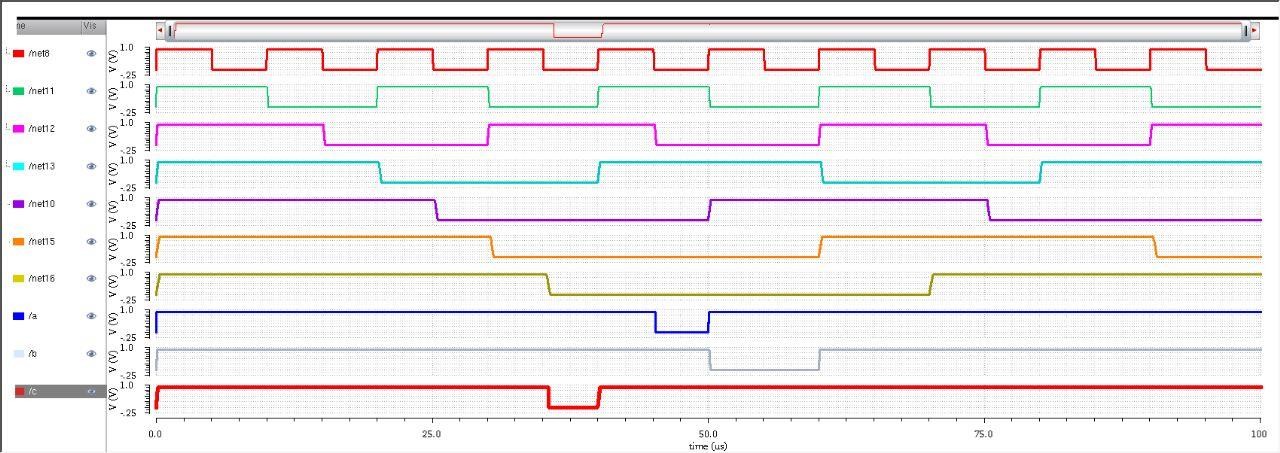
### Priority Encoder (8:3)



Schematic of Priority Encoder (8:3)

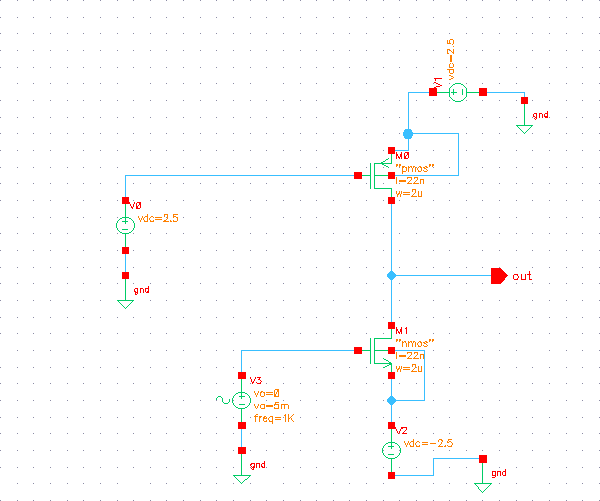


Priority Encoder Simulation using CMOS for 22nm technology.

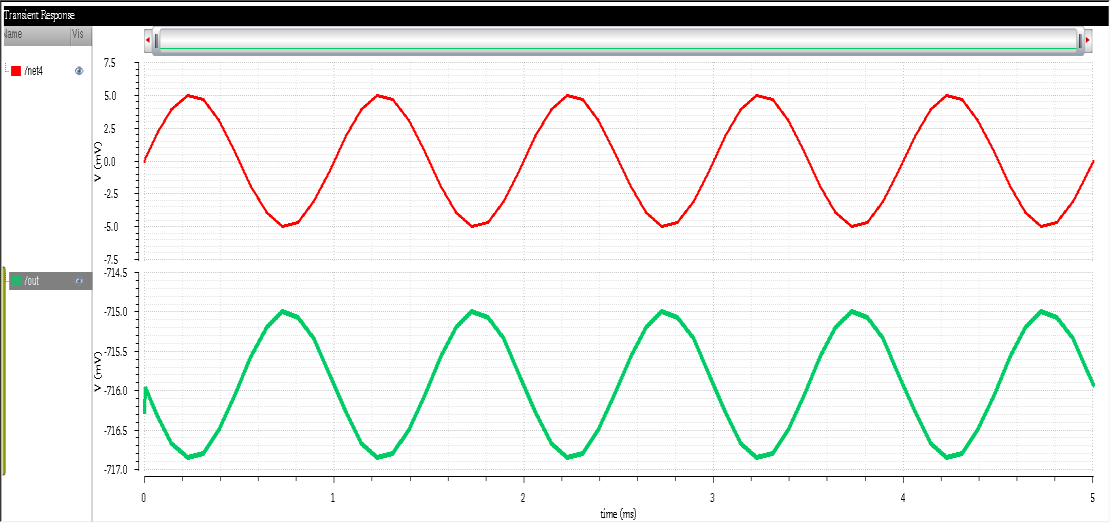


Priority Encoder simulation using FinFET for 22nm technology.

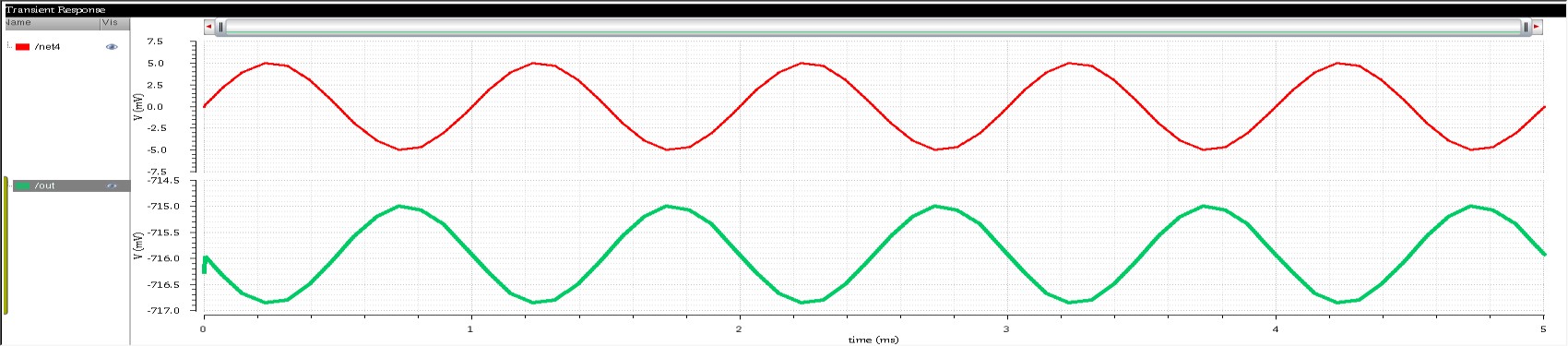
### Common Source Amplifier



Common source amplifier schematic

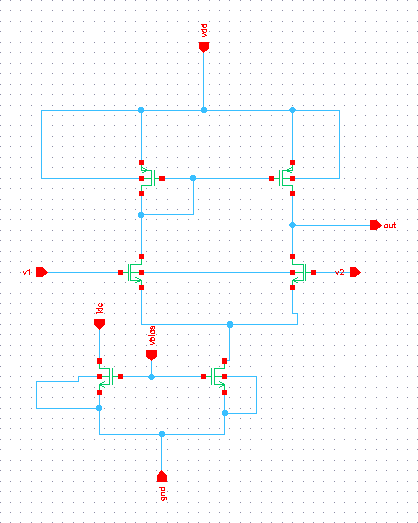


Common source amplifier simulation using CMOS for 22nm technology

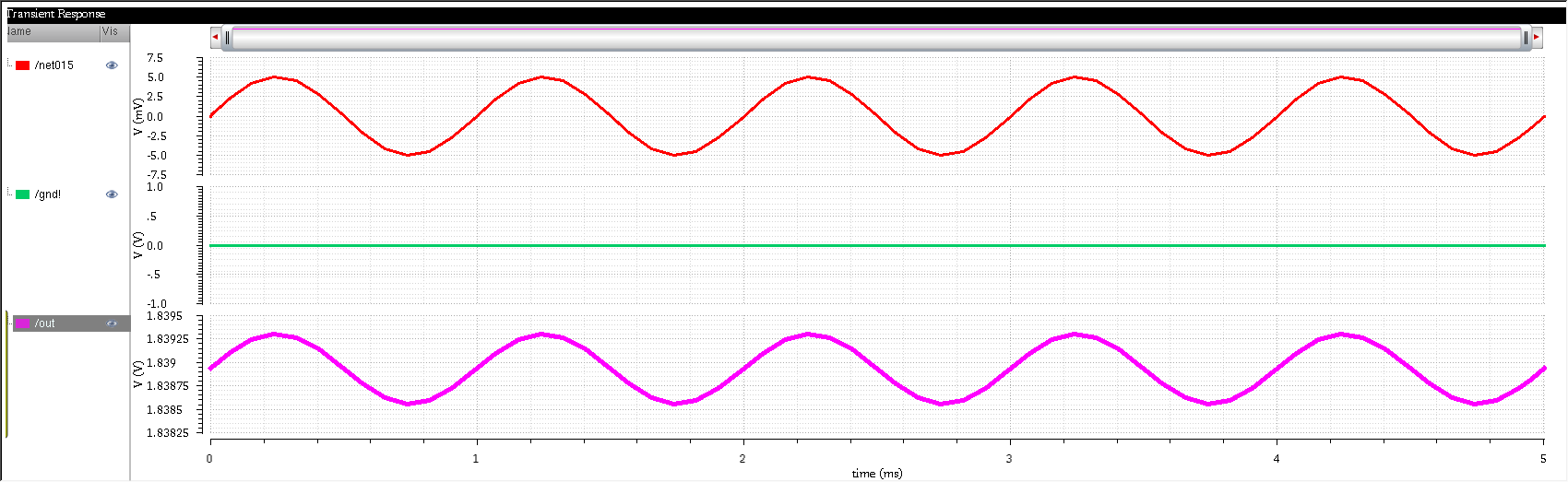


Common source amplifier simulation using FinFET for 22nm technology

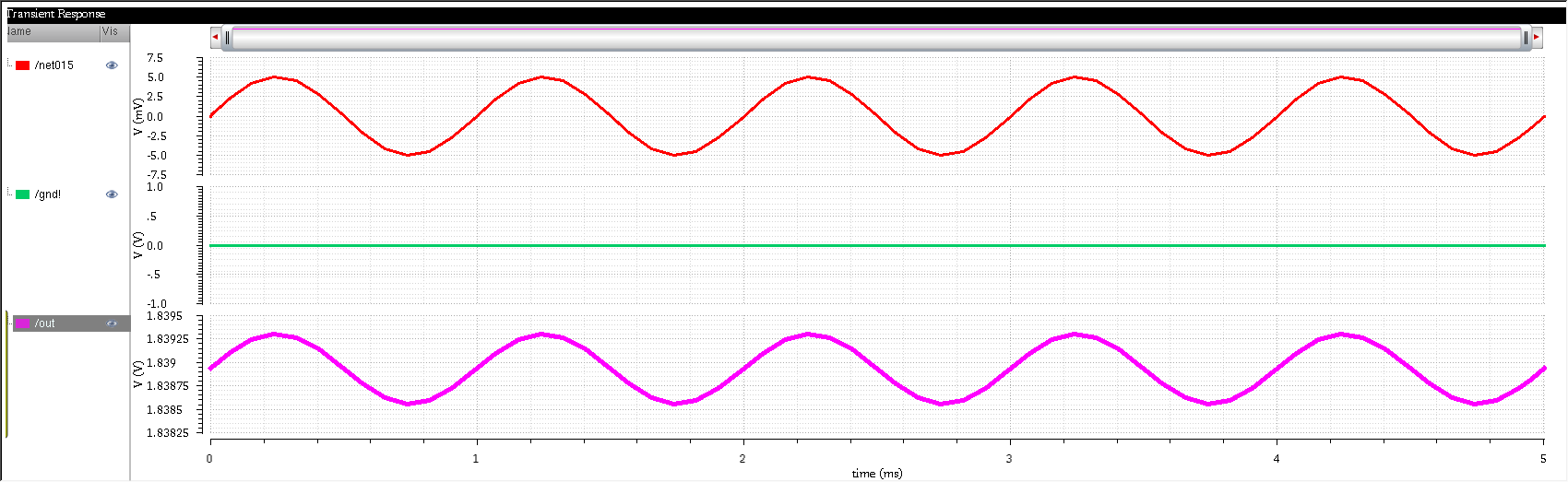
### Differential Amplifier



Differential Amplifier schematic



Differential amplifier simulation using CMOS for 22nm technology



Differential amplifier simulation using FinFET for 22nm technology

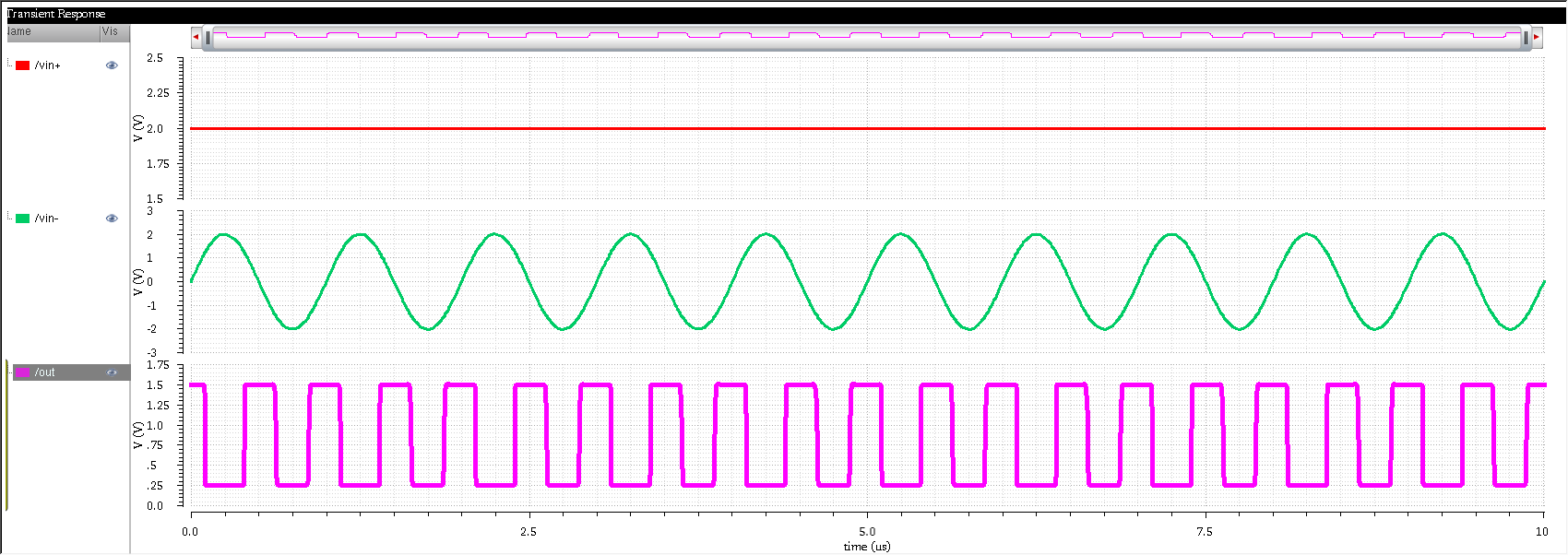
## Comparator

## 

Comparator



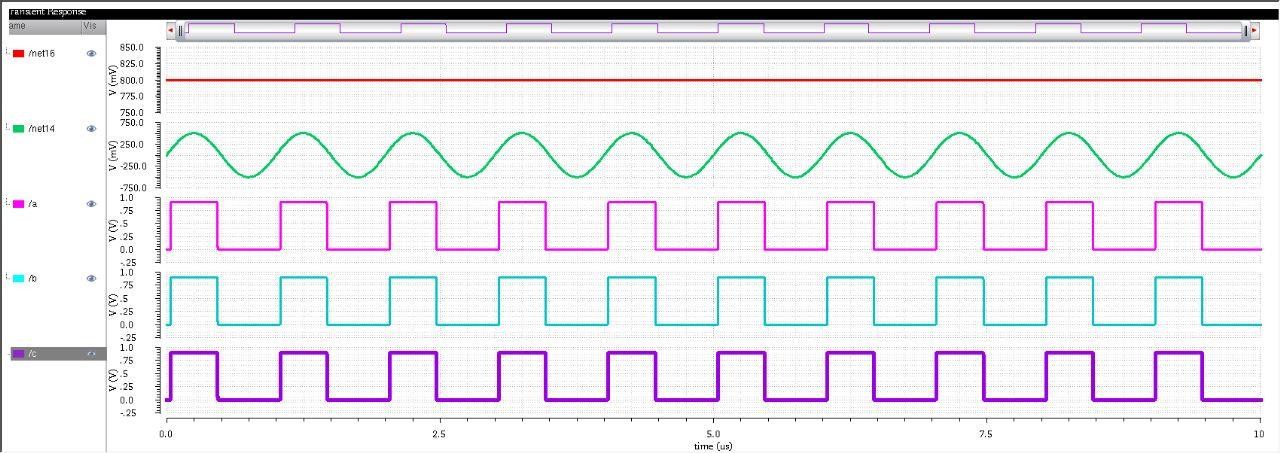
Comparator simulation using CMOS for 22nm technology



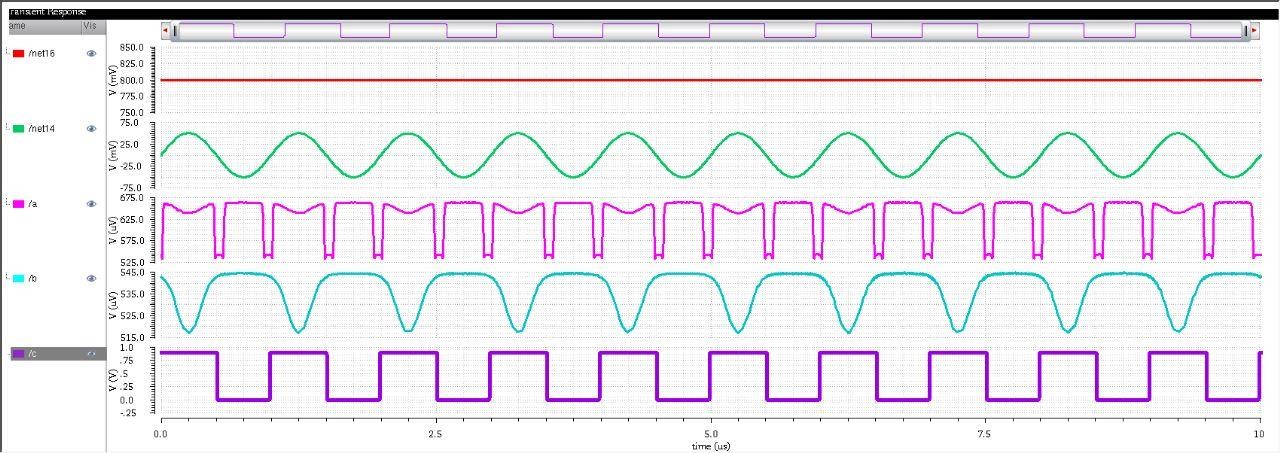
Comparator simulation using FinFET for 22nm technology

## 3-bit Flash ADC

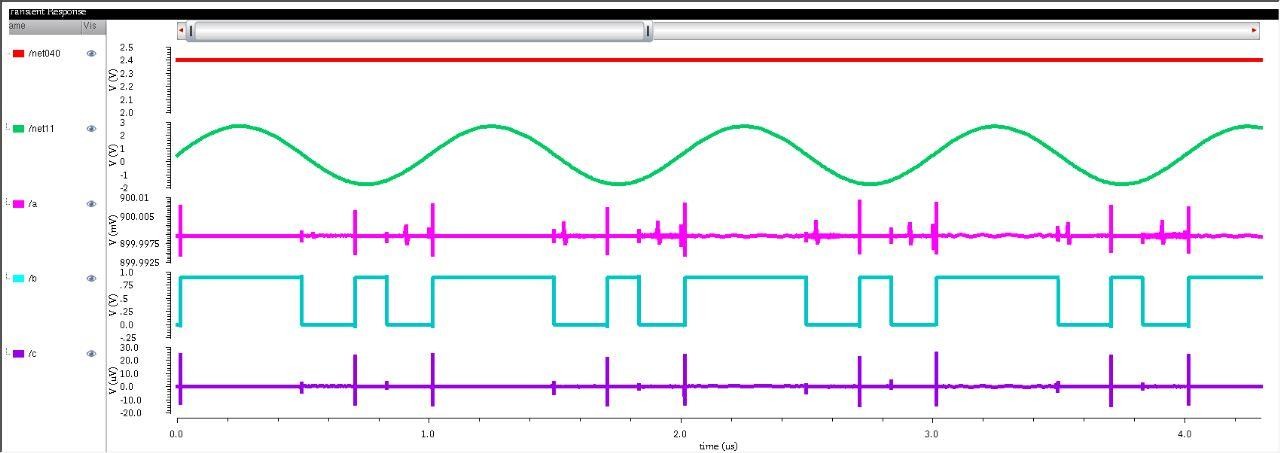
## 

 3-bit Flash ADC

3-bit flash ADC simulation using CMOS for 22nm technology



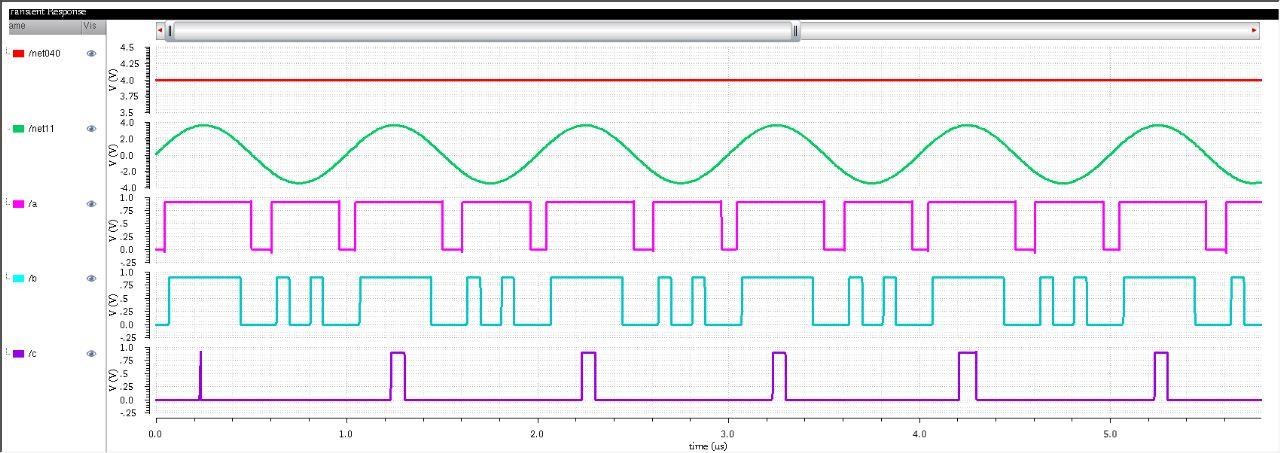
3-bit flash ADC simulation using CMOS for 22nm technology



3-bit flash ADC simulation using FinFET for 22nm technology

Code transitions for Flash ADC

|  |  |  |
| --- | --- | --- |
| Vin | code | a b c |
| 0<vin≤0.3 | 0000000 | 000 |
| 0.3<vin≤0.6 | 0000001 | 001 |
| 0.6<vin≤0.9 | 0000011 | 010 |
| 0.9<vin≤1.2 | 0000111 | 011 |
| 1.2<vin≤1.5 | 0001111 | 100 |
| 1.5<vin≤1.8 | 0011111 | 101 |
| 1.8<vin≤2.1 | 0111111 | 110 |
| 2.1<vin | 1111111 | 111 |



3-bit flash ADC simulation using FinFET for 22nm technology

Code transitions for Flash ADC

|  |  |  |
| --- | --- | --- |
| Vin | code | a b c |
| 0<vin≤0.5 | 0000000 | 000 |
| 0.5<vin≤1 | 0000001 | 001 |
| 1<vin≤1.5 | 0000011 | 010 |
| 1.5<vin≤2 | 0000111 | 011 |
| 2<vin≤2.5 | 0001111 | 100 |
| 2.5<vin≤3 | 0011111 | 101 |
| 3<vin≤3.5 | 0111111 | 110 |
| 3.5<vin | 1111111 | 111 |



3-bit flash ADC simulation using FinFET for 22nm technology

Code transitions for Flash ADC

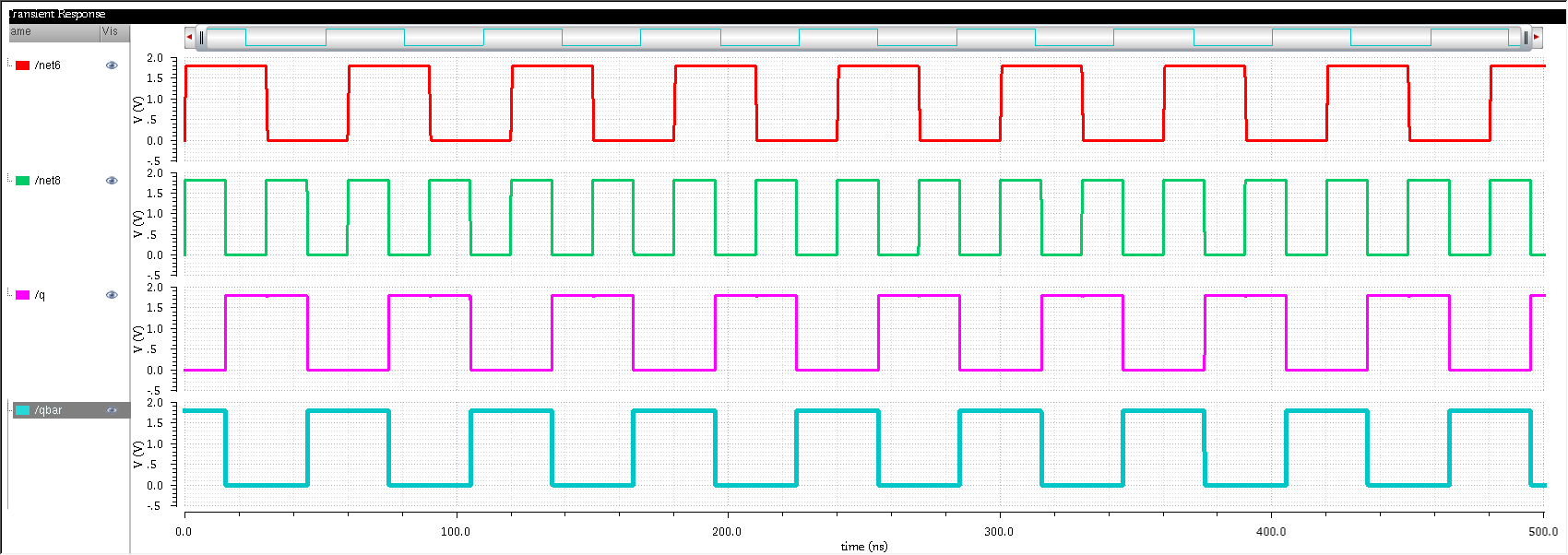
|  |  |  |
| --- | --- | --- |
| Vin | code | a b c |
| 0<vin≤0.2 | 0000000 | 000 |
| 0.2<vin≤0.4 | 0000001 | 001 |
| 0.4<vin≤0.6 | 0000011 | 010 |
| 0.6<vin≤1.8 | 0000111 | 011 |
| 0.8<vin≤1 | 0001111 | 100 |
| 1.0<vin≤1.2 | 0011111 | 101 |
| 1.2<vin≤1.4 | 0111111 | 110 |
| 1.4<vin | 1111111 | 111 |

### D Flip-Flop

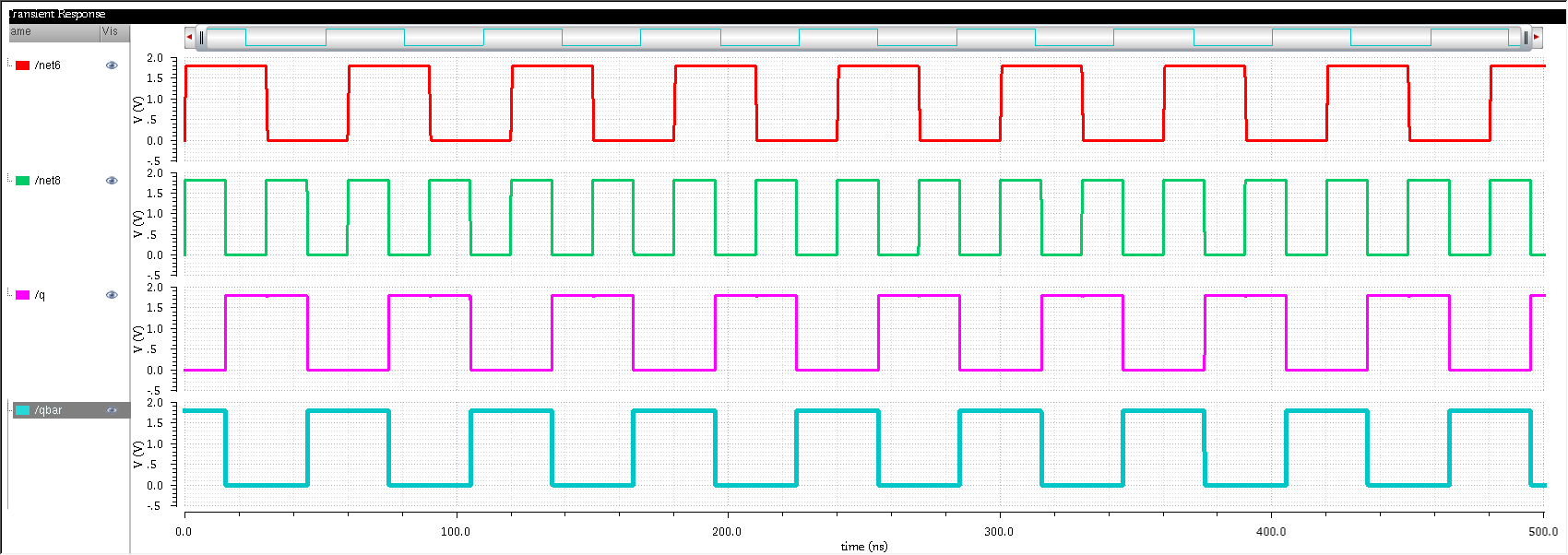
### 

Figure 5.1.6(a): D Flip-Flop

D Flip-Flop



D Flip-Flop simulation using CMOS for 22nm technology



D Flip-Flop simulation using FinFET for 22nm technology

### Johnson Counter

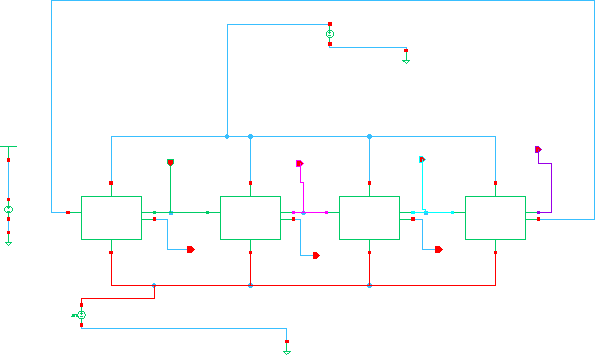
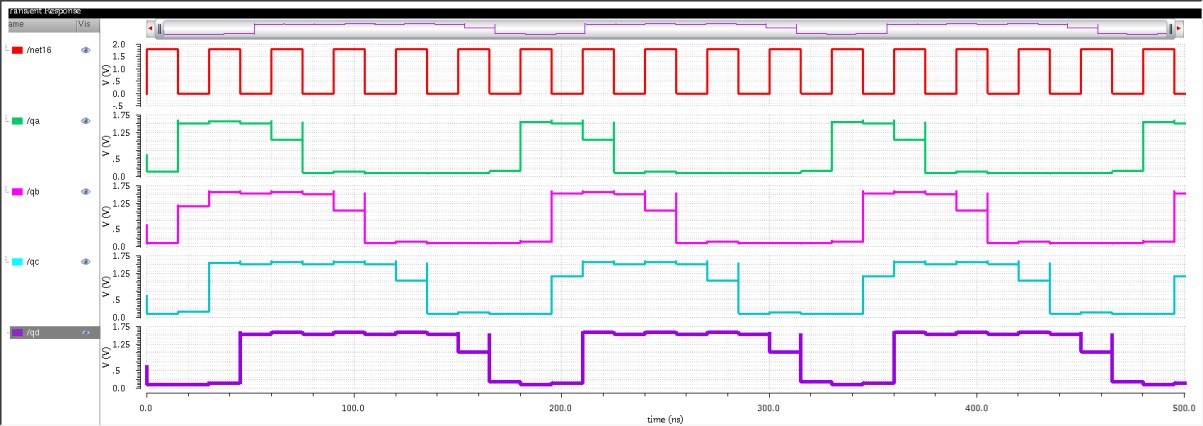
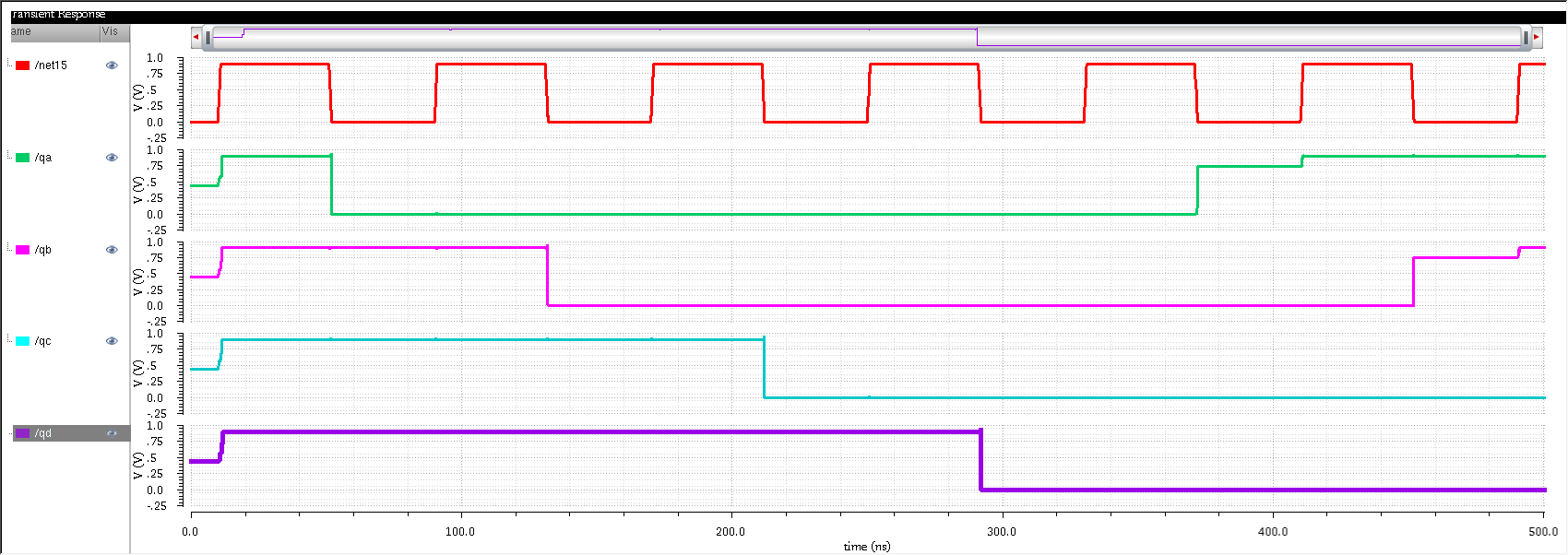


Figure 5.1.7(a): Johnson Counter

Johnson Counter



Johnson Counter simulation using CMOS for 22nm technology



Johnson Counter simulation using FinFET for 22nm techn